What is claimed is:

1. A method for power gating a downlink beam frame signal, the method comprising:

transmitting, to form a single frame, at least a first header signal, a first payload signal, a second header signal, and a second payload signal;

when a power gating signal is active, removing RF power from at least one of the first header signal and first payload signal in combination, and the second header signal and second payload signal in combination, thereby reducing DC power consumption.

2. The method of claim 1, further comprising hopping the downlink beam frame signal between at least two terrestrial cells.

3. The method of claim 2, further comprising the step of activating the power gating signal based on the terrestrial cell to which the downlink beam frame signal is currently hopped.

4. The method of claim 1, further comprising the step of activating the power gating signal based on a statistical multiplexing estimate of downlink frame utilization.

5. The method of claim 1, further comprising the step of activating the power gating signal in order to maintain at least one data queue on average approximately at preselected occupancy level.

6. The method of claim 1, further comprising the step of transmitting a first flush signal and a second flush signal, and wherein removing power comprises removing power from at least one of the first header signal, first payload signal, and first flush signal in combination, and the second header signal, second payload signal, and second flush signal in combination.

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7. The method of claim 1, wherein removing power for the first header signal, the first payload signal, the second header signal, and the second payload signal.

8. The method of claim 1, wherein removing power comprises removing power from the first payload signal, the second header signal, and the second payload signal.

9. The method of claim 1, wherein removing power comprises removing power from the first header signal, the first payload signal, and the second payload signal.

10. The method of claim 1, wherein transmitting comprises transmitting to form a single frame a first header signal, a first payload signal, a second header signal, a second payload signal, at least one additional header signal, and at least one additional payload signal;

when the power gating signal is active, removing power from at least one of the first header signal and first payload signal in combination, the second header signal and second payload signal in combination, and the additional header signal and the additional payload signal in combination.

11. A power gating module for power gating a downlink beam frame signal, the power gating module comprising:

a power amplifier for amplifying for transmission frame signals including at least a first header signal, a first payload signal, a second header signal, and a second payload signal;

a power gating circuit coupled to the power amplifier, the power gating circuit including a power gate input and responsive to a power gating signal to remove power from at least one of the first header signal and first payload signal in combination, and the second header signal and second payload signal in combination before amplification by the power amplifier.

12. The power gating module of claim 11, wherein the power gating circuit comprises a digital modulator with a gating control input connected to the power gate input and a bandpass filter with a predetermined passband coupled to a modulator output of the digital modulator.

13. The power gating module of claim 12, wherein the digital modulator outputs a modulated signal with frequency content outside the passband in response to the power gating signal.

14. The power gating module of claim 13, wherein the frequency content is substantially DC frequency content.

15. The power gating module of claim 12, wherein the digital modulator is a QPSK modulator and further comprising an Inphase gate and a Quadrature gate coupled to the digital modulator.

16. The power gating module of claim 15, wherein the Inphase gate and the Quadrature gate are held in a known output state in response to the power gating signal.

17. The power gating module of claim 11, wherein the power gating signal is active during the first header signal, the first payload signal, the second header signal, and the second payload signal.

18. The power gating module of claim 11, wherein the power gating signal is active during the first payload signal, the second header signal, and the second payload signal.

19. The power gating module of claim 11, wherein the power gating signal is active during the first header signal, the first payload signal, and the second payload signal.

20. The power gating module of claim 11, comprising:

a switch coupled to the power amplifier, the switch including a feed path selection input;

a first feed path coupled to the switch and characterized by a first hop location; and

a second feed path coupled to the switch and characterized by a second hop location.

21. The power gating module of claim 20, wherein the switch is a ferrite switch.

22. The power gating module of claim 20, wherein the power gating signal is active based in part on the feed path selection of the first hop location or the second hop location.

23. A power gated frame signal comprising:

a single frame comprising at least a first header signal, a first payload signal, a second header signal, and a second payload signal,

wherein at least one of the first header signal and first payload signal in combination, and the second header signal and second payload signal in combination is power gated.

24. The power gated frame signal of claim 23, wherein the single frame further comprises at least one additional header signal, and at least one additional payload signal, and

wherein at least one of the first header signal and first payload signal in combination, the second header signal and second payload signal in combination, and the additional header signal and the

additional payload signal in combination is power gated.

25. The power gating module of claim 23, wherein the first header signal, the first payload signal, the second header signal, and the second payload signal are power gated.

26. The power gating module of claim 23, wherein the first payload signal, the second header signal, and the second payload signal are power gated.

27. The power gating module of claim 23, wherein the first header signal, the first payload signal, and the second payload signal are power gated.

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